What is claimed is:

1. A wiring board comprising:

an insulating board defined by a first surface and a second surface opposing to the first surface;

a plurality of first signal strips disposed selectively on the first surface;

a first power distribution plane provided on the first surface so as to occupy a residual area of the first signal strips, disposing spaces along both sides of the first signal strips such that the first signal strips are electrically isolated from the first power distribution planes;

a plurality of lands disposed on the second surface;

a plurality of via metals penetrating the insulating board so as to electrically connect the lands to the corresponding first signal strips respectively; and

a second power distribution plane provided on the second surface so as to occupy a residual area of the lands, disposing spaces along the lands such that the lands are electrically isolated from the second distribution plane.

2. The wiring board of claim 1, further comprising a plurality of second signal strips disposed on the second surface, connecting the lands to the corresponding via metals respectively, disposing spaces along both sides of the second signal strips such that the second signal

strips are electrically isolated from the second power distribution plane.

3. The wiring board of claim 1, wherein a plurality of the first power distribution planes are arranged in mirror symmetry about the center line of the first surface.

4. The wiring board of claim 1, wherein each of the spacings between the first power distribution plane and the first signal strips is 30 μm to 120 μm.

5. The wiring board of claim 1, wherein the first and second power distribution planes have different electric potentials.

6. The wiring board of claim 1, wherein the first power distribution plane delivers a high power supply voltage and the second power distribution plane delivers a low power supply voltage.

7. The wiring board of claim 1, wherein the first signal strips and the lands are mutually arranged in a topology such that the positions of the lands do not face to the route of the first signal strips, being isolated by the wiring board.

8. The wiring board of claim 7, wherein the first signal

strips have bends to avoid facing to the positions of the lands.

9. The wiring board of claim 1, wherein each of the first signal strips has a wiring pad portion protruded from a side defining a part of the contour of an area occupied by the first power distribution plane at an end of the corresponding first signal strip, opposing to the other end connected to the corresponding via metal.

10. The wiring board of claim 9, wherein the first power distribution plane has a power pad portion protruded in the same direction with the wiring pad portion at the side of the first power distribution plane.

11. A packaging assembly comprising:

an insulating board defined by a first surface and a second surface opposing to the first surface;

a plurality of first signal strips disposed selectively on the first surface;

a first power distribution plane provided on the first surface so as to occupy a residual area of the first signal strips, disposing spaces along both sides of the first signal strips such that the first signal strips are electrically isolated from the first power distribution planes;

a plurality of lands disposed on the second surface;

a plurality of via metals penetrating the insulating board so as to electrically connect the lands to the corresponding first signal strips respectively;

a second power distribution plane provided on the second surface so as to occupy a residual area of the lands, disposing spaces along the lands such that the lands are electrically isolated from the second distribution plane; and

a semiconductor chip disposed on the first surface connected to a plurality of the pad potion formed at the end of the first signal strips and the first power distribution plane.

12. The packaging assembly of claim 11, further comprising a plurality of second signal strips disposed on the second surface, connecting the lands to the corresponding via metals respectively, disposing spaces along both sides of the second signal strips such that the second signal strips are electrically isolated from the second power distribution plane.

13. The packaging assembly of claim 11, wherein a plurality of the first power distribution planes are arranged in mirror symmetry about the center line of the first surface.

14. The packaging assembly of claim 11, wherein each of the spacings between the first power distribution plane and the first signal strips is 30 μm to 120 μm.

15. The packaging assembly of claim 11, wherein the first and second power distribution planes have different electric potentials.

16. The packaging assembly of claim 11, wherein the first power distribution plane delivers a high power supply voltage and the second power distribution plane delivers a low power supply voltage.

17. The packaging assembly of claim 11, wherein the first signal strips and the lands are mutually arranged in a topology such that the positions of the lands do not face to the route of the first signal strips, being isolated by the wiring board.

18. The packaging assembly of claim 11, wherein the first signal strips have bends to avoid facing to the positions of the lands.

19. The packaging assembly of claim 11, wherein the semiconductor chip is disposed between two pieces of the first power distribution planes disposed separately.

20. The packaging assembly of claim 11, wherein the pad portion includes a wiring pad portion protruded from a side defining a part of the contour of an area occupied by the first power distribution plane at an end of the corresponding first signal strip, opposing to the other end connected to the corresponding via metal, and a power pad portion protruded in the same direction with the wiring pad portion at the side of the first power distribution plane.

21. The packaging assembly of claim 20, wherein the semiconductor chip is mounted face down on the first surface.